Lattice Semiconductor Corporation

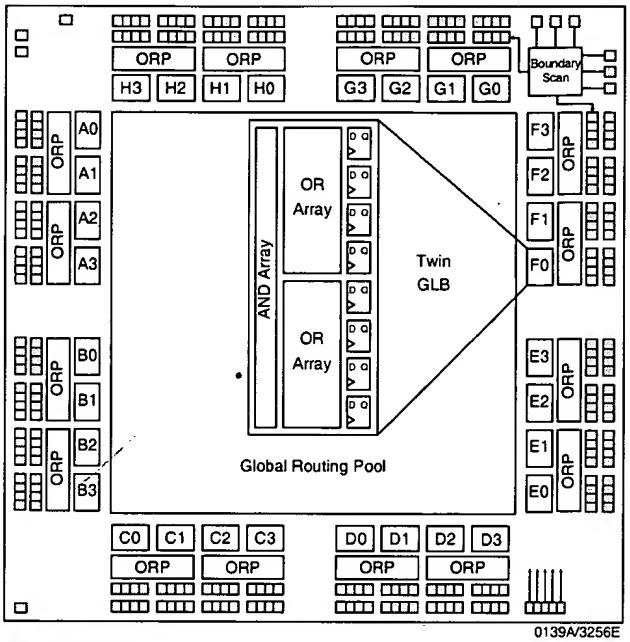
ispLSI® 3256E

In-System Programmable High Density PLD

Features

- **HIGH-DENSITY PROGRAMMABLE LOGIC**
  - — 256 I/O Pins
  - — 12000 PLD Gates
  - — 512 Registers
  - — High Speed Global Interconnect
  - — Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
  - — Small Logic Block Size for Random Logic
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - — f_{max} = 100 MHz Maximum Operating Frequency
  - — t_{pd} = 10 ns Propagation Delay
  - — TTL Compatible Inputs and Outputs
  - — Electrically Erasable and Reprogrammable
  - — Non-Volatile
  - — 100% Tested at Time of Manufacture
  - — Unused Product Term Shutdown Saves Power
- **IN-SYSTEM PROGRAMMABLE**
  - — 5V In-System Programmable (ISP™) using Lattice ISP or Boundary Scan Test (IEEE 1149.1) Protocol
  - — Increased Manufacturing Yields, Reduced Time-to-Market, and Improved Product Quality
  - — Reprogram Soldered Devices for Faster Debugging
- **100% IEEE 1149.1 BOUNDARY SCAN COMPATIBLE**
- **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - — Complete Programmable Device Can Combine Glue Logic and Structured Designs
  - — Five Dedicated Clock Input Pins
  - — Synchronous and Asynchronous Clocks
  - — Programmable Output Slew Rate Control to Minimize Switching Noise
  - — Flexible Pin Placement
  - — Optimized Global Routing Pool Provides Global Interconnectivity
- **ispDesignEXPERT™ – LOGIC COMPILER AND COMPLETE ISP DEVICE DESIGN SYSTEMS FROM HDL SYNTHESIS THROUGH IN-SYSTEM PROGRAMMING**
  - — Superior Quality of Results
  - — Tightly Integrated with Leading CAE Vendor Tools
  - — Productivity Enhancing Timing Analyzer, Explore Tools, Timing Simulator and ispANALYZER™
  - — PC and UNIX Platforms

Functional Block Diagram



0139A/3256E

Description

The ispLSI 3256E is a High Density Programmable Logic Device containing 512 Registers, 256 Universal I/O pins, five Dedicated Clock Input Pins, 16 Output Routing Pools (ORP) and a Global Routing Pool (GRP) which allows complete inter-connectivity between all of these elements. The ispLSI 3256E features 5V in-system programmability and in-system diagnostic capabilities. The ispLSI 3256E offers non-volatile reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems.

The basic unit of logic on the ispLSI 3256E device is the Twin Generic Logic Block (Twin GLB) labelled A0, A1...H3. There are a total of 32 Twin GLBs in the ispLSI 3256E device. Each Twin GLB has 24 inputs, a programmable AND array and two OR/Exclusive-OR Arrays and eight outputs which can be configured to be either combinatorial or registered. All Twin GLB inputs come from the GRP.

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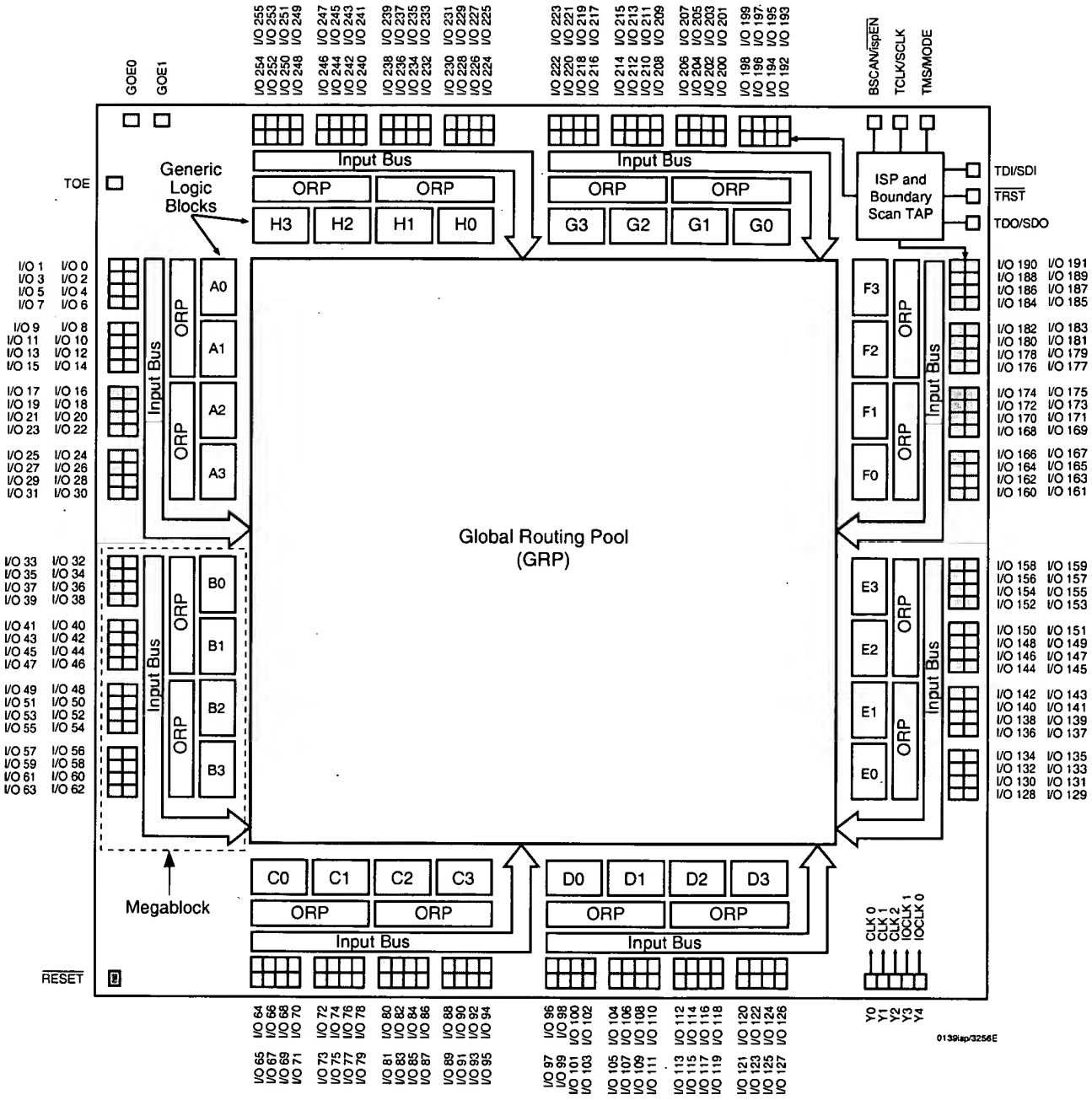
Functional Block Diagram

Figure 1. ispLSI 3256E Functional Block Diagram



Description (continued)

All local logic block outputs are brought back into the GRP so they can be connected to the inputs of any other logic block on the device. The device also has 256 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, a registered input, a latched input, an output or a bidirectional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise.

The 256 I/O Cells are grouped into 16 sets of 16 bits. Pairs of these I/O groups are associated with a logic Megablock through the use of the ORP. Each Megablock is able to provide one Product Term Output Enable (PTOE) signal which is globally distributed to all I/O cells. That PTOE signal can be generated within any GLB in the Megablock. Each I/O cell can select either a Global OE or a PTOE.

Four Twin GLBs, 32 I/O Cells and two ORPs are connected together to make a logic Megablock. The Megablock is defined by the resources that it shares. The outputs of the four Twin GLBs are connected to a set of 32 I/O cells by the ORP. The ispLSI 3256E device contains eight of these Megablocks.

The GRP has as its inputs the outputs from all of the Twin GLBs and all of the inputs from the bidirectional I/O cells. All of these signals are made available to the inputs of the Twin GLBs. Delays through the GRP have been equalized to minimize timing skew and logic glitching.

Clocks in the ispLSI 3256E device are provided through five dedicated clock pins. The five pins provide three clocks to the Twin GLBs and two clocks to the I/O cells.

The table below lists key attributes of the device along with the number of resources available.

An additional feature of the ispLSI 3256E is its Boundary Scan capability, which is composed of cells connected between the on-chip system logic and the device's input and output pins. All I/O pins have associated boundary scan registers, with 3-state I/O using three boundary scan registers and inputs using one.

The ispLSI 3256E supports all IEEE 1149.1 mandatory instructions, which include BYPASS, EXTEST and SAMPLE.

Key Attributes of the ispLSI 3256E

Attribute	Quantity
Twin GLBs	32
Registers	512
I/O Pins	256
Global Clocks	5
Global OE	2
Test OE	1

Table - 003/3256E

Absolute Maximum Ratings [1]

Supply Voltage V_{CC} ..... -0.5 to +7.0V

Input Voltage Applied ..... -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied (304-Pin PQFP) ..... 150°C

Max. Junction Temp. (T_J) with Power Applied (320-Ball BGA) ..... 140°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Condition

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	70	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	0	0.8	V
V_{IH}	Input High Voltage	2.0	V_{CC} +1	V

Table 2-0005/3256E

Capacitance (T_A=25°C,f=1.0 MHz)

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_1	I/O Capacitance	10	pf	V_{CC}= 5.0V, $V_{I/O}$ = 2.0V
C_2	Clock Capacitance	15	pf	V_{CC}= 5.0V, V_Y = 2.0V

Table 2-0006/3256E

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	Years
ispLSI Erase/Reprogram Cycles	10000	–	Cycles

Table 2-0008/3256E

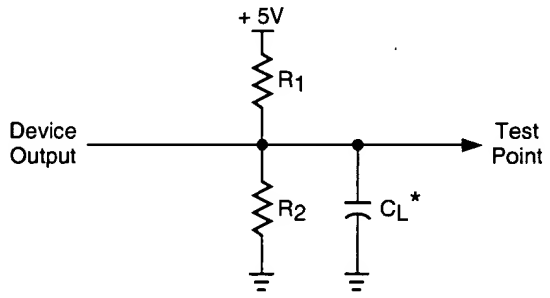
Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure 2

Table 2-0003/3256E

3-state levels are measured 0.5V from steady-state active level.

Figure 2. Test Load



*C_L includes Test Fixture and Probe Capacitance.

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Output Load conditions (See Figure 2)

TEST CONDITION		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH}-0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL}+0.5V	470Ω	390Ω	5pF

Table 2 - 0004A

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL}= 8 mA	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH}= -4 mA	2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (Max.)	–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}	–	–	10	µA
I_{IL-isp}	Bscan/$\overline{ispEN}$ Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL}	–	–	-150	µA
I_{IL-PU}	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}	–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC}= 5V, V_{OUT}= 0.5V	–	–	-200	mA
I_{CC}[2,4]	Operating Power Supply Current	V_{IL}= 0.0V, V_{IH}= 3.0V f_{TOGGLE}= 1 MHz	–	300	–	mA

Table 2 - 0007isp/3256E

1. One output at a time for a maximum duration of one second. V_{OUT}= 0.5V was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.
2. Measured using sixteen 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this datasheet and Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM to estimate maximum I_{CC}.

External Switching Characteristics[1, 2, 3]

Over Recommended Operating Conditions

PARAMETER	TEST[5] COND.	#[2]	DESCRIPTION[1]	-100		-70		UNITS
				MIN.	MAX.	MIN.	MAX.	
tpd1	A	1	Data Prop. Delay, 4PT Bypass, ORP Bypass	—	10.0	—	15.0	ns
tpd2	A	2	Data Propagation Delay	—	13.0	—	18.0	ns
fmax	A	3	Clock Frequency with Internal Feedback[3]	100	—	70.0	—	MHz
fmax (Ext.)	—	4	Clock Freq. with Ext. Feedback,1/(tsu2 + tco1)	77.0	—	50.0	—	MHz
fmax (Tog.)	—	5	Clock Frequency, Max Toggle[4]	100	—	83.0	—	MHz
tsu1	—	6	GLB Reg. Setup Time before Clock, 4PT bypass	5.5	—	9.0	—	ns
tco1	A	7	GLB Reg. Clock to Output Delay, ORP bypass	—	6.5	—	9.0	ns
th1	—	8	GLB Reg. Hold Time after Clock, 4PT bypass	0.0	—	0.0	—	ns
tsu2	—	9	GLB Reg. Setup Time before Clock	6.5	—	11.0	—	ns
tco2	—	10	GLB Reg. Clock to Output Delay	—	7.0	—	10.0	ns
th2	—	11	GLB Reg. Hold Time after Clock	0.0	—	0.0	—	ns
tr1	A	12	Ext. Reset Pin to Output Delay	—	13.5	—	15.0	ns
trw1	—	13	Ext. Reset Pulse Duration	6.5	—	12.0	—	ns
tptoeen	B	14	Input to Output Enable	—	16.0	—	19.0	ns
tptoedis	C	15	Input to Output Disable	—	16.0	—	19.0	ns
tgoeen	B	16	Global OE Output Enable	—	9.0	—	12.0	ns
tgoedis	C	17	Global OE Output Disable	—	9.0	—	12.0	ns
ttoeen	—	18	Test OE Output Enable	—	12.0	—	15.0	ns
ttoedis	—	19	Test OE Output Disable	—	12.0	—	15.0	ns
twh	—	20	Ext. Sync. Clock Pulse Duration, High	5.0	—	6.0	—	ns
twl	—	21	Ext. Sync. Clock Pulse Duration, Low	5.0	—	6.0	—	ns
tsu3	—	22	I/O Reg. Setup Time before Ext. Sync. Clock (Y3, Y4)	4.5	—	5.0	—	ns
th3	—	23	I/O Reg. Hold Time after Ext. Sync. Clock (Y3, Y4)	0.0	—	0.0	—	ns

1. Unless noted otherwise, all parameters use 20 PTXOR path and ORP.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions section.

Timing Ext.3256E.eps

Internal Timing Parameters[1]

Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-100		-70		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
tiobp	24	I/O Register Bypass	—	2.4	—	4.0	ns
tiolat	25	I/O Latch Delay	—	10.3	—	14.0	ns
tiosu	26	I/O Register Setup Time before Clock	4.8	—	5.8	—	ns
tioh	27	I/O Register Hold Time after Clock	-1.6	—	-2.5	—	ns
tioco	28	I/O Register Clock to Out Delay	—	5.8	—	8.5	ns
tior	29	I/O Register Reset to Out Delay	—	5.8	—	7.5	ns
GRP							
tgrp	30	GRP Delay	—	2.3	—	3.2	ns
GLB							
t4ptbp	31	4 Product Term Bypass Path Delay (Comb.)	—	3.2	—	3.6	ns
t4ptbr	32	4 Product Term Bypass Path Delay (Reg.)	—	3.1	—	4.8	ns
t1ptxor	33	1 Product Term/XOR Path Delay	—	4.0	—	5.1	ns
t20ptxor	34	20 Product Term/XOR Path Delay	—	4.1	—	5.2	ns
txoradj	35	XOR Adjacent Path Delay[3]	—	4.3	—	5.7	ns
tgbp	36	GLB Register Bypass Delay	—	1.5	—	1.6	ns
tgsu	37	GLB Register Setup Time before Clock	0.3	—	1.2	—	ns
tgh	38	GLB Register Hold Time after Clock	5.0	—	7.6	—	ns
tgco	39	GLB Register Clock to Output Delay	—	1.6	—	3.0	ns
tgro	40	GLB Register Reset to Output Delay	—	5.2	—	5.2	ns
tptre	41	GLB Product Term Reset to Register Delay	—	4.0	—	4.4	ns
tptoe	42	GLB Product Term Output Enable to I/O Cell Delay	—	6.5	—	6.9	ns
tptck	43	GLB Product Term Clock Delay	3.0	3.6	3.4	4.2	ns
ORP							
torp	44	ORP Delay	—	1.2	—	1.9	ns
torpbp	45	ORP Bypass Delay	—	0.7	—	0.9	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

Timing Int.3256E.eps

Internal Timing Parameters[1]

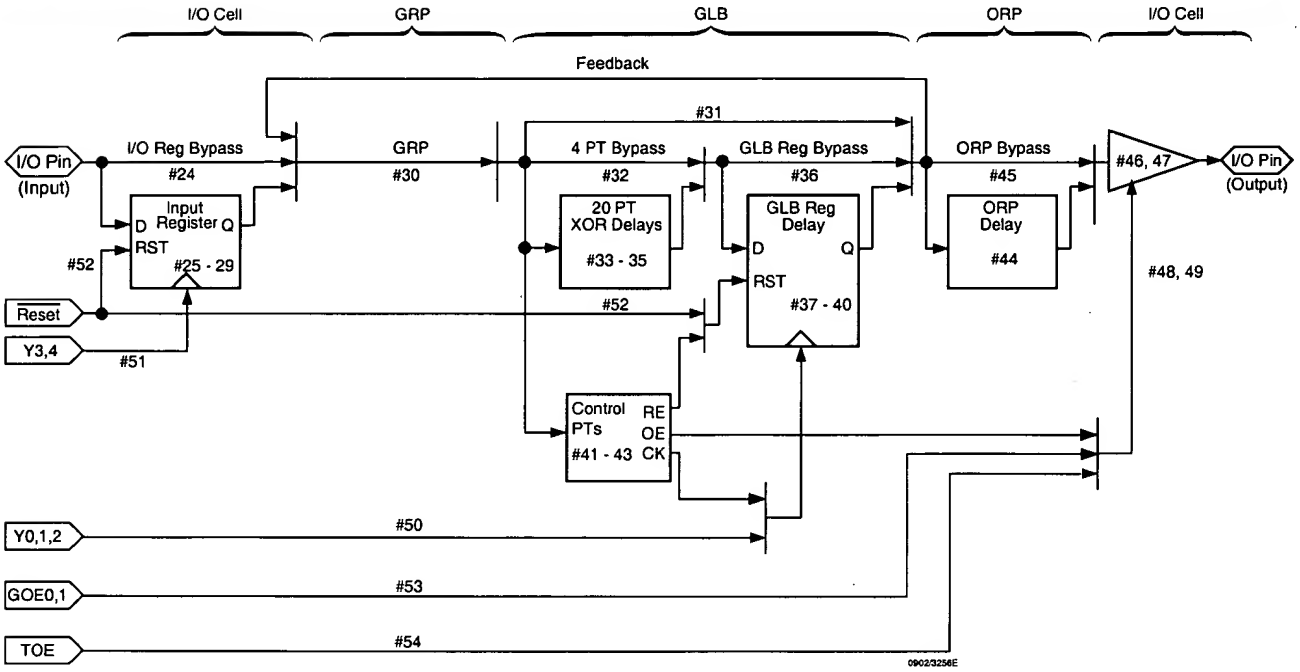
Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-100		-70		UNITS
			MIN.	MAX.	MIN.	MAX.	
Outputs							
tob	46	Output Buffer Delay	—	2.6	—	3.3	ns
tobs	47	Output Buffer Delay, Slew Limited Adder	—	17.6	—	18.3	ns
toen	48	I/O Cell OE to Output Enabled	—	5.5	—	5.7	ns
todis	49	I/O Cell OE to Output Disabled	—	5.5	—	5.7	ns
Clocks							
tgy0/1/2	50	Clock Delay, Y0 or Y1 or Y2 to Global GLB Clk Line	1.6	1.6	1.8	1.8	ns
tioy3/4	51	Clock Delay, Y3 or Y4 to I/O Cell Global Clock Line	0.3	1.6	0.8	2.5	ns
Global Reset							
tgr	52	Global Reset to GLB and I/O Registers	—	4.5	—	4.6	ns
tgoe	53	Global OE Pad Buffer	—	5.9	—	7.5	ns
ttoe	54	Test OE Pad Buffer	—	6.1	—	8.9	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

Timing Int.2.3256E.eps

ispLSI 3256E Timing Model



Derivations of tsu, th and tco from the Product Term Clock[1]

tsu = Logic + Reg su - Clock (min)
= (tiobp + tgrp + t20ptxor) + (tgsu) - (tiobp + tgrp + tptck(min))
= (#24+ #30+ #34) + (#37) - (#24+ #30+ #43)
1.4 ns = (2.4 + 2.3 + 4.1) + (0.3) - (2.4 + 2.3 + 3.0)

th = Clock (max) + Reg h - Logic
= (tiobp + tgrp + tptck(max)) + (tgh) - (tiobp + tgrp + t20ptxor)
= (#24+ #30+ #43) + (#38) - (#24+ #30+ #34)
4.5 ns = (2.4 + 2.3 + 3.6) + (5.0) - (2.4 + 2.3 + 4.1)

tco = Clock (max) + Reg co + Output
= (tiobp + tgrp + tptck(max)) + (tgco) + (torp + tob)
= (#24 + #30 + #43) + (#39) + (#44 + #46)
13.7 ns = (2.4 + 2.3 + 3.6) + (1.6) + (1.2 + 2.6)

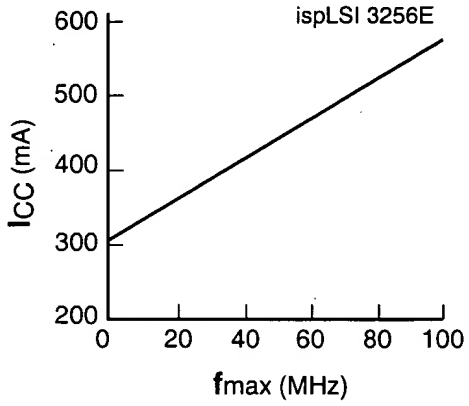
Table 2- 0042-3256E

Note: Calculations are based upon timing specifications for the ispLSI 3256E-100L.

Power Consumption

Power consumption in the ispLSI 3256E device depends on two primary factors: the speed at which the device is operating and the number of product terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of 16 16-bit Counters
Typical Current at 5V, 25° C

I_{CC} can be estimated for the ispLSI 3256E using the following equation:

I_{CC} = 60 + (# of PTs * 0.48) + (# of nets * Max. freq * 0.0106) where:
# of PTs = Number of Product Terms used in design
# of nets = Number of Signals used in device
Max. freq = Highest Clock Frequency to the device

The I_{CC} estimate is based on typical conditions (V_{CC} = 5.0V, room temperature) and an assumption of two GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

0127/3256E

Pin Description

Pin Name	Description
I/O	Input/Output pins – These are the general purpose I/O pins used by the logic array.
GOE0, GOE1	Global Output Enable input pins.
TOE	Test Output Enable pin – This pin tristates all I/O pins when a logic low is driven.
$\overline{\text{RESET}}$	Active Low (0) Reset pin – Resets all of the GLB and I/O registers in the device.
Y0, Y1, Y2	Dedicated Clock inputs. These clock inputs are connected to one of the clock inputs of all the GLBs on the device.
Y3, Y4	Dedicated Clock inputs. These clock inputs are connected to one of the clock inputs of all the I/O cells on the device.
BSCAN/$\overline{\text{ispEN}}$	Input – Dedicated in-system programming enable input pin. When this pin is high, the BSCAN TAP controller pins TMS, TDI, TDO and TCK are enabled. When this pin is brought low, the ISP State Machine control pins MODE, SDI, SDO and SCLK are enabled. High-to-low transition of this pin will put the device in the programming mode and put all I/O pins in the high-Z state.
TDI/SDI	Input – This pin performs two functions. It is the Test Data input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI is also used as one of the two control pins for the ISP State Machine.
TCK/SCLK	Input – This pin performs two functions. It is the Test Clock input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register.
TMS/MODE	Input – This pin performs two functions. It is the Test Mode Select input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a pin to control the operation of the ISP State Machine.
$\overline{\text{TRST}}$/NC[1]	Input – Test Reset, active low to reset the Boundary Scan State Machine.
TDO/SDO	Output – This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as the pin to read the ISP data. When $\overline{\text{ispEN}}$ is high, it functions as Test Data Out.
GND	Ground (GND)
VCC	Vcc
NC[1]	No Connect.

1. NC pins are not to be connected to any active signals, VCC or GND.

Pin Locations

Signal	304-Pin PQFP	320-Ball BGA
GOE0, GOE1	195, 185	AD11, AC14
TOE	215	AC6
$\overline{\text{RESET}}$	53	A17
Y0, Y1, Y2, Y3, Y4	43, 33, 205, 175, 165	A14, B11, AD8, AB16, AA18
$\overline{\text{ispEN}}$/BSCAN	63	B19
SDI/TDI	23	C9
SCLK/TCK	73	D20
MODE/TMS	13	D7
$\overline{\text{TRST}}$/NC[1]	225	AA5
SDO/TDO	155	AB21
GND	9, 19, 39, 49, 69, 85, 95, 115, 125, 145, 161, 171, 191, 201, 221, 237, 247, 267, 277, 297	D6, C8, B13, A16, D19, F21, H22, N23, T24, W21, AA19, AB17, AC12, AD9, AA6, W4, U3, M2, J1, F4
VCC	1, 29, 59, 77, 105, 135, 153, 181, 211, 229, 257, 287, 304	D4, B10, B18, D21, K23, V23, AA21, AC15, AC7, AA4, R2, G2, C3
NC[1]		A1, A2, A23, A24, B1, B2, B23, B24, AC1, AC2, AC23, AC24, AD1, AD2, AD23, AD24

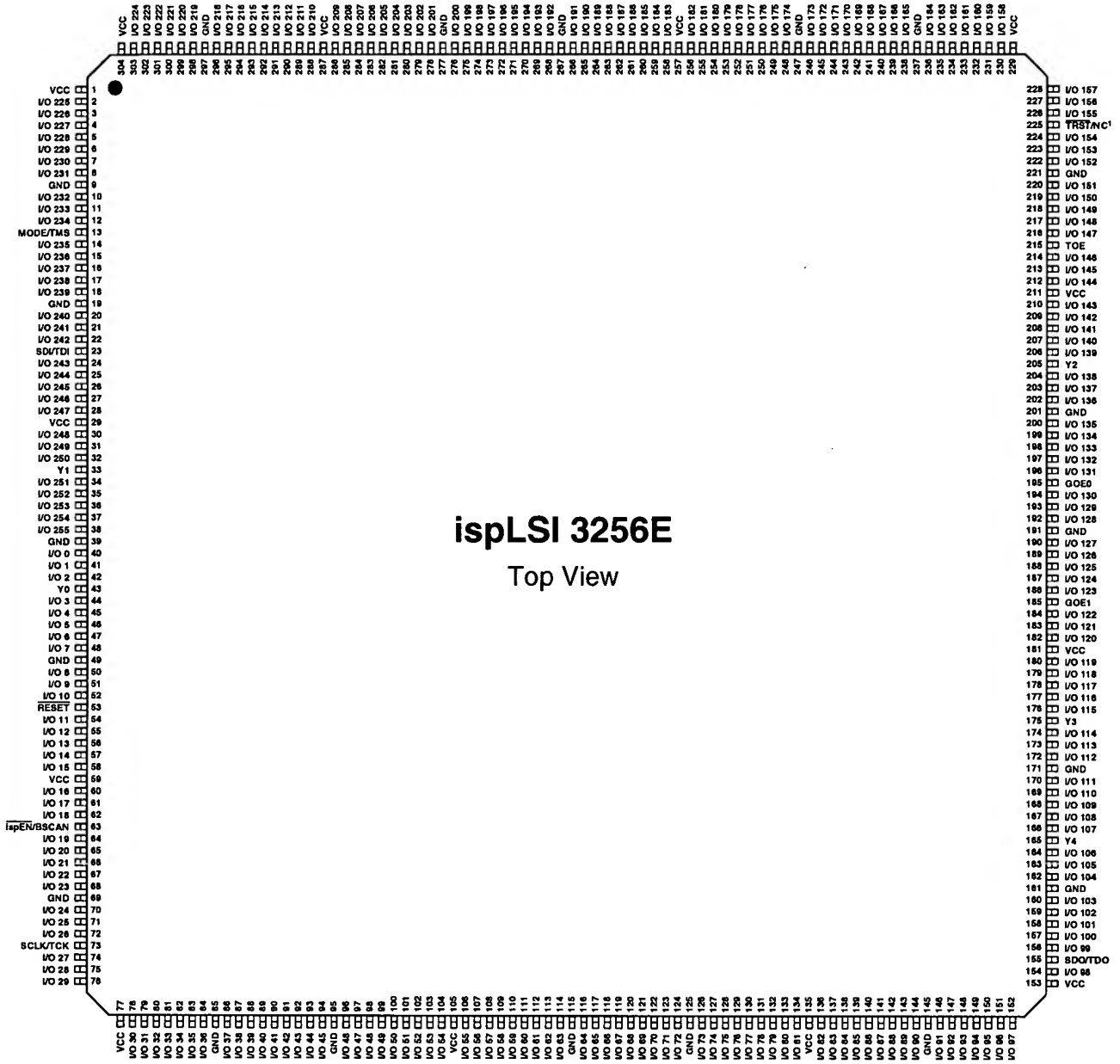
1. NC pins are not to be connected to any active signals, VCC or GND.

I/O Locations

Signal	PQFP	BGA	Signal	PQFP	BGA	Signal	PQFP	BGA	Signal	PQFP	BGA	Signal	PQFP	BGA
I/O 0	40	C13	I/O 53	103	K22	I/O 106	164	AD20	I/O 159	231	AA3	I/O 212	290	G3
I/O 1	41	D13	I/O 54	104	J24	I/O 107	166	AC19	I/O 160	232	AB1	I/O 213	291	F2
I/O 2	42	A13	I/O 55	106	K24	I/O 108	167	AB18	I/O 161	233	Y4	I/O 214	292	E1
I/O 3	44	B14	I/O 56	107	L21	I/O 109	168	AD19	I/O 162	234	AA2	I/O 215	293	G4
I/O 4	45	C14	I/O 57	108	L22	I/O 110	169	AA17	I/O 163	235	Y3	I/O 216	294	F3
I/O 5	46	D14	I/O 58	109	L23	I/O 111	170	AC18	I/O 164	236	AA1	I/O 217	295	E2
I/O 6	47	A15	I/O 59	110	L24	I/O 112	172	AD18	I/O 165	238	Y2	I/O 218	296	D1
I/O 7	48	B15	I/O 60	111	M24	I/O 113	173	AA16	I/O 166	239	W3	I/O 219	298	E3
I/O 8	50	C15	I/O 61	112	M21	I/O 114	174	AC17	I/O 167	240	Y1	I/O 220	299	D2
I/O 9	51	D15	I/O 62	113	M22	I/O 115	176	AD17	I/O 168	241	V4	I/O 221	300	C1
I/O 10	52	B16	I/O 63	114	M23	I/O 116	177	AC16	I/O 169	242	W2	I/O 222	301	E4
I/O 11	54	C16	I/O 64	116	N22	I/O 117	178	AA15	I/O 170	243	V3	I/O 223	302	D3
I/O 12	55	B17	I/O 65	117	N21	I/O 118	179	AB15	I/O 171	244	W1	I/O 224	303	C2
I/O 13	56	D16	I/O 66	118	N24	I/O 119	180	AD16	I/O 172	245	U4	I/O 225	2	B3
I/O 14	57	A18	I/O 67	119	P24	I/O 120	182	AD15	I/O 173	246	V2	I/O 226	3	C4
I/O 15	58	C17	I/O 68	120	P23	I/O 121	183	AA14	I/O 174	248	V1	I/O 227	4	A3
I/O 16	60	A19	I/O 69	121	P22	I/O 122	184	AB14	I/O 175	249	T4	I/O 228	5	D5
I/O 17	61	D17	I/O 70	122	P21	I/O 123	186	AD14	I/O 176	250	U2	I/O 229	6	B4
I/O 18	62	C18	I/O 71	123	R24	I/O 124	187	AD13	I/O 177	251	T3	I/O 230	7	C5
I/O 19	64	A20	I/O 72	124	R23	I/O 125	188	AA13	I/O 178	252	U1	I/O 231	8	A4
I/O 20	65	D18	I/O 73	126	R22	I/O 126	189	AB13	I/O 179	253	T2	I/O 232	10	B5
I/O 21	66	C19	I/O 74	127	R21	I/O 127	190	AC13	I/O 180	254	R4	I/O 233	11	C6
I/O 22	67	B20	I/O 75	128	T23	I/O 128	192	AB12	I/O 181	255	R3	I/O 234	12	A5
I/O 23	68	A21	I/O 76	129	U24	I/O 129	193	AA12	I/O 182	256	T1	I/O 235	14	B6
I/O 24	70	C20	I/O 77	130	T22	I/O 130	194	AD12	I/O 183	258	R1	I/O 236	15	C7
I/O 25	71	B21	I/O 78	131	U23	I/O 131	196	AC11	I/O 184	259	P4	I/O 237	16	A6
I/O 26	72	A22	I/O 79	132	T21	I/O 132	197	AB11	I/O 185	260	P3	I/O 238	17	D8
I/O 27	74	C21	I/O 80	133	V24	I/O 133	198	AA11	I/O 186	261	P2	I/O 239	18	B7
I/O 28	75	B22	I/O 81	134	U22	I/O 134	199	AD10	I/O 187	262	P1	I/O 240	20	A7
I/O 29	76	C22	I/O 82	136	W24	I/O 135	200	AC10	I/O 188	263	N1	I/O 241	21	D9
I/O 30	78	C23	I/O 83	137	U21	I/O 136	202	AB10	I/O 189	264	N4	I/O 242	22	B8
I/O 31	79	D22	I/O 84	138	V22	I/O 137	203	AA10	I/O 190	265	N3	I/O 243	24	A8
I/O 32	80	C24	I/O 85	139	W23	I/O 138	204	AC9	I/O 191	266	N2	I/O 244	25	B9
I/O 33	81	E21	I/O 86	140	Y24	I/O 139	206	AB9	I/O 192	268	M3	I/O 245	26	D10
I/O 34	82	D23	I/O 87	141	V21	I/O 140	207	AC8	I/O 193	269	M4	I/O 246	27	C10
I/O 35	83	E22	I/O 88	142	W22	I/O 141	208	AA9	I/O 194	270	M1	I/O 247	28	A9
I/O 36	84	D24	I/O 89	143	Y23	I/O 142	209	AD7	I/O 195	271	L1	I/O 248	30	A10
I/O 37	86	E23	I/O 90	144	AA24	I/O 143	210	AB8	I/O 196	272	L2	I/O 249	31	D11
I/O 38	87	F22	I/O 91	146	Y22	I/O 144	212	AD6	I/O 197	273	L3	I/O 250	32	C11
I/O 39	88	E24	I/O 92	147	AA23	I/O 145	213	AA8	I/O 198	274	L4	I/O 251	34	A11
I/O 40	89	G21	I/O 93	148	AB24	I/O 146	214	AB7	I/O 199	275	K1	I/O 252	35	A12
I/O 41	90	F23	I/O 94	149	Y21	I/O 147	216	AD5	I/O 200	276	K2	I/O 253	36	D12
I/O 42	91	G22	I/O 95	150	AA22	I/O 148	217	AA7	I/O 201	278	K3	I/O 254	37	C12
I/O 43	92	F24	I/O 96	151	AB23	I/O 149	218	AB6	I/O 202	279	K4	I/O 255	38	B12
I/O 44	93	H21	I/O 97	152	AB22	I/O 150	219	AC5	I/O 203	280	J2			
I/O 45	94	G23	I/O 98	154	AC22	I/O 151	220	AD4	I/O 204	281	H1			
I/O 46	96	G24	I/O 99	156	AD22	I/O 152	222	AB5	I/O 205	282	J3			
I/O 47	97	J21	I/O 100	157	AA20	I/O 153	223	AC4	I/O 206	283	H2			
I/O 48	98	H23	I/O 101	158	AC21	I/O 154	224	AD3	I/O 207	284	J4			
I/O 49	99	J22	I/O 102	159	AB20	I/O 155	226	AB4	I/O 208	285	G1			
I/O 50	100	H24	I/O 103	160	AD21	I/O 156	227	AC3	I/O 209	286	H3			
I/O 51	101	J23	I/O 104	162	AC20	I/O 157	228	AB3	I/O 210	288	F1			
I/O 52	102	K21	I/O 105	163	AB19	I/O 158	230	AB2	I/O 211	289	H4			

Pin Configuration

ispLSI 3256E 304-Pin PQFP Pinout Diagram



1. NC pins are not to be connected to any active signals, VCC or GND.

304MQFP.3256E

Signal Configuration

ispLSI 3256E 320-Ball BGA Signal Diagram

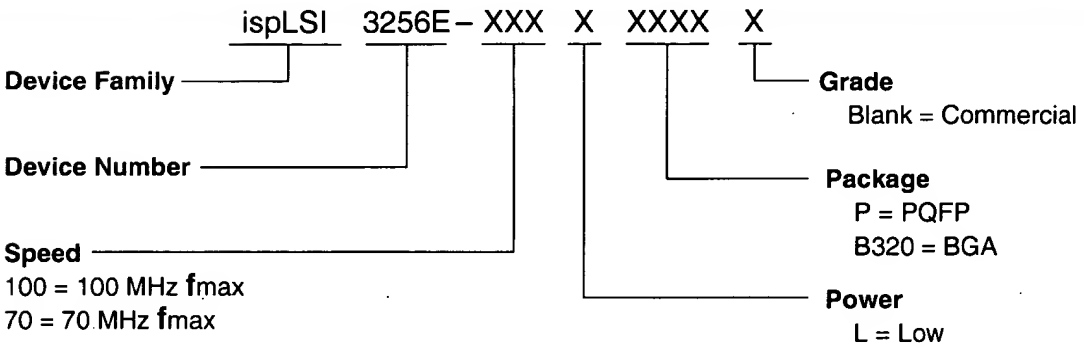
	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	NC[1]	NC[1]	I/O 26	I/O 23	I/O 19	I/O 16	I/O 14	RESET	GND	I/O 6	Y0	I/O 2	I/O 252	I/O 251	I/O 248	I/O 247	I/O 243	I/O 240	I/O 237	I/O 234	I/O 231	I/O 227	NC[1]	NC[1]	A
B	NC[1]	NC[1]	I/O 28	I/O 25	I/O 22	ispEN/ BSCAN	VCC	I/O 12	I/O 10	I/O 7	I/O 3	GND	I/O 255	Y1	VCC	I/O 244	I/O 242	I/O 239	I/O 235	I/O 232	I/O 229	I/O 225	NC[1]	NC[1]	B
C	I/O 32	I/O 30	I/O 29	I/O 27	I/O 24	I/O 21	I/O 18	I/O 15	I/O 11	I/O 8	I/O 4	I/O 0	I/O 254	I/O 250	I/O 246	SDI/ TDI	GND	I/O 236	I/O 233	I/O 230	I/O 226	VCC	I/O 224	I/O 221	C
D	I/O 36	I/O 34	I/O 31	VCC	SCLK/ TCK	GND	I/O 20	I/O 17	I/O 13	I/O 9	I/O 5	I/O 1	I/O 253	I/O 249	I/O 245	I/O 241	I/O 238	MODE/ TMS	GND	I/O 228	VCC	I/O 223	I/O 220	I/O 218	D
E	I/O 39	I/O 37	I/O 35	I/O 33																	I/O 222	I/O 219	I/O 217	I/O 214	E
F	I/O 43	I/O 41	I/O 38	GND																	GND	I/O 216	I/O 213	I/O 210	F
G	I/O 46	I/O 45	I/O 42	I/O 40																	I/O 215	I/O 212	VCC	I/O 208	G
H	I/O 50	I/O 48	GND	I/O 44																	I/O 211	I/O 209	I/O 206	I/O 204	H
J	I/O 54	I/O 51	I/O 49	I/O 47																	I/O 207	I/O 205	I/O 203	GND	J
K	I/O 55	VCC	I/O 53	I/O 52																	I/O 202	I/O 201	I/O 200	I/O 199	K
L	I/O 59	I/O 58	I/O 57	I/O 56																	I/O 198	I/O 197	I/O 196	I/O 195	L
M	I/O 60	I/O 63	I/O 62	I/O 61																	I/O 193	I/O 192	GND	I/O 194	M
N	I/O 66	GND	I/O 64	I/O 65																	I/O 189	I/O 190	I/O 191	I/O 188	N
P	I/O 67	I/O 68	I/O 69	I/O 70																	I/O 184	I/O 185	I/O 186	I/O 187	P
R	I/O 71	I/O 72	I/O 73	I/O 74																	I/O 180	I/O 181	VCC	I/O 183	R
T	GND	I/O 75	I/O 77	I/O 79																	I/O 175	I/O 177	I/O 179	I/O 182	T
U	I/O 76	I/O 78	I/O 81	I/O 83																	I/O 172	GND	I/O 176	I/O 178	U
V	I/O 80	VCC	I/O 84	I/O 87																	I/O 168	I/O 170	I/O 173	I/O 174	V
W	I/O 82	I/O 85	I/O 88	GND																	GND	I/O 166	I/O 169	I/O 171	W
Y	I/O 86	I/O 89	I/O 91	I/O 94																	I/O 161	I/O 163	I/O 165	I/O 167	Y
AA	I/O 90	I/O 92	I/O 95	VCC	I/O 100	GND	Y4	I/O 110	I/O 113	I/O 117	I/O 121	I/O 125	I/O 129	I/O 133	I/O 137	I/O 141	I/O 145	I/O 148	GND	TRST/ NC[1]	VCC	I/O 159	I/O 162	I/O 164	AA
AB	I/O 93	I/O 96	I/O 97	SDO/ TDO	I/O 102	I/O 105	I/O 108	GND	Y3	I/O 118	I/O 122	I/O 126	I/O 128	I/O 132	I/O 136	I/O 139	I/O 143	I/O 146	I/O 149	I/O 152	I/O 155	I/O 157	I/O 158	I/O 160	AB
AC	NC[1]	NC[1]	I/O 98	I/O 101	I/O 104	I/O 107	I/O 111	I/O 114	I/O 116	VCC	GOE 1	I/O 127	GND	I/O 131	I/O 135	I/O 138	I/O 140	VCC	TOE	I/O 150	I/O 153	I/O 156	NC[1]	NC[1]	AC
AD	NC[1]	NC[1]	I/O 99	I/O 103	I/O 106	I/O 109	I/O 112	I/O 115	I/O 119	I/O 120	I/O 123	I/O 124	I/O 130	GOE 0	I/O 134	GND	Y2	I/O 142	I/O 144	I/O 147	I/O 151	I/O 154	NC[1]	NC[1]	AD
	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

ispLSI 3256E
Bottom View

1. NC pins are not to be connected to any active signals, VCC or GND.

Note: Ball A1 indicator dot on top side of package.

Part Number Description



0212/3256E

Ordering Information

COMMERCIAL

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	100	10	ispLSI 3256E-100LQ	304-Pin PQFP
	100	10	ispLSI 3256E-100LB320	320-Ball BGA
	70	15	ispLSI 3256E-70LQ	304-Pin PQFP
	70	15	ispLSI 3256E-70LB320	320-Ball BGA

Table 2-0041/3256E